## IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

Please replace the paragraph on page 1, commencing on line 32, with the following amended paragraph:

To perform the required signal processing, some conventional receiver units are designed with a number of processing elements, with each processing element being designed especially for, and dedicated to perform, a specific function. For example, a receiver unit may be designed with a searcher element and a number of data processing elements. The searcher element searches the received signal for strong signal instances, and the data processing elements are assigned to process specific signal instances of sufficient signal strength. Implementation of multiple parallel processing elements results in increased circuit complexity and costs. The processing elements are also typically of fixed designs, and no programmability is typically provided (e.g., to ~~processed~~ process the received signal with different sets of parameter values to perform, for example, pilot processing, signal searches, and data demodulation). Moreover, the number of signal instances that can be processed is limited to the number of processing elements implemented.

Please replace the paragraph on page 5, commencing on line 6, with the following amended paragraph:

The controller can be designed to maintain a timing state machine for each signal instance being processed. Each timing state machine can be maintained using DSP (digital signal processor) firmware, and may include a time tracking loop used to (1) track movement of the signal instance being processed and (2) generate a time offset corresponding to the signal instance. The time offset can be used to retrieve the proper segment of samples from the first buffer to process. The controller can further receive a timing signal, which is used to initiate processing of the segments of samples. The timing signal can be generated based on a comparison value provided by the controller.

Please replace the paragraph on page 7, commencing on line 23, with the following amended paragraph:

Communications system 100 can be a code division multiple access (CDMA) system or other multiple access communications system that supports voice and data communication between users over a terrestrial link. The use of CDMA techniques in a multiple access communications system is disclosed in U.S. Patent No. 4,901,307, entitled "SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS," and U.S. Patent No. 5,103,459, entitled "SYSTEM AND METHOD FOR GENERATING WAVEFORMS IN A CDMA CELLULAR TELEPHONE ~~SYSTEM,".~~ SYSTEM." Another specific CDMA system is disclosed in U.S. Patent Application Serial No. 08/963,386, entitled "METHOD AND APPARATUS FOR HIGH RATE PACKET DATA TRANSMISSION," filed November 3, 1997, now U.S. Patent No. 6,574,211, issued June 3, 2003 to Padovani et al. These patents and patent application are assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph on page 8, commencing on line 21, with the following amended paragraph:

Depending on the particular design of receiver unit 200, ADCs 216 may provide $I_{ADC}$ and $Q_{ADC}$ samples at a high sample rate and corresponding to signals received from one or more antennas. Data interface circuit 222 may decimate (i.e., remove) unnecessary samples, ~~arranges~~ arrange (i.e., ~~sorts~~ sort) samples corresponding to each antenna, and ~~assembles~~ assemble the samples into words suitable for efficient storage to a buffer 224. In a specific embodiment, each word comprises 32 bits of data, each $I_{ADC}$ or $Q_{ADC}$ sample comprises 4 bits of data, and four pairs of $I_{ADC}$ and $Q_{ADC}$ samples are arranged into each word. Other word widths (e.g., 16 bits, 64 bits, 128 bits, and so on) may also be used and are within the scope of the invention. When a word is available for storage, a data write address DW_ADDR is generated by an address generator 220, and the word is written to buffer 224 at the location identified by the generated data write address.

Please replace the paragraph on page 10, commencing on line 13, with the following amended paragraph:

In an embodiment, address generator 220 ~~include~~ includes a data write address generator that generates the data write address DW_ADDRESS and a data read address generator that generates a data read address DR_ADDR. Address generator 220 may further include address generators for other data (PN sequences) that may also be stored in buffer 224. In an embodiment, address generator 236 ~~include~~ includes a symbol write address generator that generates the symbol write address SW_ADDRESS and a symbol read address generator that generates the symbol read address SR_ADDR. Address generators 220 and 236 are described in further detail below.

Please replace the paragraph on page 10, commencing on line 28, with the following amended paragraph:

First, data processor 230 performs many of the computationally intensive operations and thus allows controller 240 to support many users concurrently. Data processor 230 can be designed to perform the required processing on the received data and to provide demodulated symbols directly to decoder 260. Controller 240 can thus be relieved of the intensive data processing (e.g., dot product computation), which typically equates to the need for a more complicated controller in conventional designs and traditionally prevents the controller from concurrently supporting a number of users or processing a number of signal instances. Moreover, micro-controller 232 can be provided to perform the "micro-management" of data processor 230 and to relieve controller 240 of some of the mundane management duties.

Please replace the paragraph on page 12, commencing on line 3, with the following amended paragraph:

FIG. 3 is a diagram of a data frame format for the forward link transmission in accordance with the HDR CDMA system. On the forward link, traffic data, pilot reference, and signaling data are time division multiplexed in a frame and transmitted from a base station to a particular user terminal. Each frame covers a time unit referred to as a slot (e.g., 1.67 for a particular design of the HDR system). Each slot includes traffic data fields 302a, 302b, and

302c, pilot reference fields 304a and 304b, and signaling data i.e., overhead (OH) fields 306a and 306b. Traffic data fields 302 and pilot reference fields 304 are used to send traffic data and pilot reference, respectively. Signaling data fields 306 are used to send signaling information such as, for example, forward link activity (FAC) indicators, reverse link busy indicators, reverse link power control commands, and so on. The FAC indicators indicate whether the base station has traffic data to send a particular number of slots in the future. The reverse link busy indicators indicate whether the reverse link capacity limit of the base station has been reached. And the power control commands direct transmitting user terminals to increase or decrease their transmit power.

Please replace the paragraph on page 14, commencing on line 9, with the following amended paragraph:

The design and operation of a rake receiver for [[an]] a CDMA system is described in further detail in U.S. Patent No. 5,764,687, entitled "MOBILE DEMODULATOR ARCHITECTURE FOR A SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM," and U.S. Patent No. 5,490,165, entitled "DEMODULATION ELEMENT ASSIGNMENT IN A SYSTEM CAPABLE OF RECEIVING MULTIPLE SIGNALS." Pilot carrier dot product and the (optimal) weighting of the rake receiver finger paths are described in further detail in U.S. Patent No. 5,506,865, entitled "PILOT CARRIER DOT PRODUCT CIRCUIT." The patents are assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph on page 14, commencing on line 19, with the following amended paragraph:

In the HDR CDMA system, power control data for a particular user terminal is covered with a particular Walsh code assigned to the terminal and transmitted in each slot. Thus, within data correlator 410, the despread $I_{DES}$ and $Q_{DES}$ samples are decovered by Walsh decover element 442 with the assigned Walsh code. The decovered power control samples are then provided to an accumulator 444 and accumulated over the duration of a power control burst to generate a power control bit for the signal instance being processed. The power control

bits from all assigned data correlators 410 may be coherently combined (not shown in FIG. 4 for simplicity) to ~~generated~~ generate a combined power control bit that is then used to adjust the transmit power of the user terminal.

Please replace the paragraph on page 15, commencing on line 16, with the following amended paragraph:

Data processor 230 can be directed to process the data samples in accordance with a particular set of parameter values. For traffic data processing, data processor 230 may be directed to: (1) despread and decover a particular instance of the received signal at a particular time offset, (2) perform pilot demodulation of the decovered symbols, and (3) coherently combine demodulated symbols corresponding to different signal instances, and so on. For signaling (e.g., pilot and power control) data processing, data processor 230 may be directed to: (1) despread and/or decover a particular instance of the received signal, (2) accumulate the decovered samples over a particular time interval, (3) combine accumulated symbols from various signal instances, and so on. Data processor 230 may also be operated to search for strong instances of the received signal. Data processor 230 can be designed and operated to ~~performed~~ perform various signal processing, depending on the particular CDMA standard or system and the particular (forward or reverse link) data transmission being supported.

Please replace the second paragraph on page 16, commencing on line 11, with the following amended paragraph:

In the embodiment shown in FIG. 5, the I and Q samples from buffer 224 are provided to a correlator 522 within data processor 230. Correlator 522 further receives the complex PN despreading sequence, which may also be stored in buffer 224 or generated by a PN generator (not shown in FIG. 5). For traffic data processing, correlator 522 despreads the I and Q samples with the complex PN despreading sequence to provide despread samples. Correlator 522 thus performs the despreading function performed by complex multiplier 412 in FIG. 4. Correlator [[524]] 522 may also be designed to perform other functions such as, for example, accumulation of multiple despread samples for each chip interval, interpolation of the despread

samples, and so on. The despread samples are provided to a symbol demodulator and combiner 524.

Please replace the paragraph on page 17, commencing on line 11, with the following amended paragraph:

For signaling data processing, correlator 522 can be configured to despread the I and Q samples with the complex PN despreading sequence and provide the despread samples to an accumulator 526. Accumulator 526 may be configured to decover the despread samples with one or more Walsh codes, ~~accumulates~~ accumulate the despread or decovered samples over a particular time period (e.g., a pilot reference period), and ~~provides~~ provide the recovered (e.g., pilot or power control) data to controller 240. Accumulator 526 may also be configured to provide processed samples used to search for strong instances of the received signal at various time offsets, as described below.

Please replace the paragraph on page 21, commencing on line 23, with the following amended paragraph:

As noted above, the samples are stored to buffer 224 starting at a designated location in memory at an arbitrary point in time. As a result, the starting samples for each signal instance being processed can correspond to any location in buffer 224. In an embodiment, the time tracking loop 634 is used to determine the starting location of the received data packet for each signal instance being processed. The time tracking loop 634 processes the received samples to determine a particular time offset for the received signal instance. This time offset is then used to generate the starting address for each segment of samples to be processed.

Please replace the paragraph on page 21, commencing on line 32, with the following amended paragraph:

State machines 630 can be implemented by controller 240 using DSP firmware and with a basic set of processing elements. For example, a single time tracking loop 634 and a

single data/PN address calculation unit 636 can be time division multiplexed and used to implement all instantiated state machines 630. Controller 240 can maintain a separate register to store the time offset associated with each instantiated state ~~machines~~ machine 630.

Please replace the last paragraph on page 21, commencing on line 38, with the following amended paragraph:

In an embodiment, for the forward link processing in a remote terminal, controller 240 also maintains a frequency tracking loop 638 that locks the frequency of the clock source to the data rate of the data samples. The frequency tracking loop can be designed to determine the amount of phase rotation in the pilot references, use the phase information to determine whether the sampling clock is fast or slow relative to the chip rate, and adjust the frequency of the clock source accordingly. If the sampling clock is frequency locked to the chip rate, a particular number of data samples (e.g., 2048) are provided for each frame. Thus, when the frequency is locked, a frame of samples can be deemed to be received by counting the number of samples being written to buffer 224.

Please replace the paragraph on page 23, commencing on line 1, with the following amended paragraph:

In many communications systems including the HDR CDMA system, interleaving is used to provide temporal diversity in the transmitted data. The interleaving reduces the likelihood of receiving a ~~sting~~ string of consecutive errors due to, for example, impulse noise. At the receiver unit, the received symbols are reordered. The reordering can effectively spread a string of symbols received in error over an entire frame, which can improve the likelihood of correct decoding of the received symbols. The interleaving is performed at the transmitter unit such that temporal diversity is achieved prior to the decoding at the receiver unit.

Please replace the paragraph on page 23, commencing on line 10, with the following amended paragraph:

In an embodiment, buffer/de-interleaver 234 is also operated to provide de-interleaving of the processed symbols. In an embodiment, the processed symbols are written to buffer/de-interleaver 234 [[is]] in sequential order but are read out in a pseudo-random but deterministic order defined by the particular interleaving scheme being implemented. Because the symbols are read out in non-sequential order, buffer/de-interleaver 234 is first filled with the symbols corresponding to the duration over which interleaving is performed. For example, in the HDR CDMA system, interleaving is performed on each frame of data. Thus, at the receiver unit, a complete frame of symbols is processed and stored to buffer/de-interleaver 234. After the entire frame has been processed, the symbols for the frame are read out to the subsequent decoder. In an embodiment, data processing is performed on one frame of data at a time. In this manner, as the current frame is being processed and stored to one section of buffer/de-interleaver 234, the prior processed frame can be retrieved from another section of buffer/de-interleaver 234.

Please replace the last paragraph on page 25, commencing on line 31, with the following amended paragraph:

Referring back to FIG. 7A, the despread $I_{DES}$ and $Q_{DES}$ samples from multipliers 720a through 720d are selectively combined by summers 722a through 722d to generate a set of combined $I_C$ and $Q_C$ samples. Specifically, summer 722a combines the despread $I_{DES}$ samples from multipliers 720a and 720c to generate the first combined $I_{C1}$ sample corresponding to the first half of a chip, summer 722b combines the despread $I_{DES}$ samples from multipliers 720b and 720d to generate the second combined $I_{C2}$ sample corresponding to the second half of a chip, summer 722c combines the despread $Q_{DES}$ samples from multipliers 720a and 720c to generate the first combined $Q_{C1}$ sample, and summer 722d combines the despread $Q_{DES}$ samples from multipliers ~~720a and 720c~~ 720b and 720d to generate the second combined $Q_{C2}$ sample. Summers 722 can be used to combine half samples from different chips before the interpolation, to simplify the design of the interpolator. AND gates 718 and the ZERO_0 and ZERO_1 signals can be used to disable the summing of samples from two chips when this is not applicable, such

as in the forward link symbol demodulation where each chip may contain a complex or higher order modulated symbol.

Please replace the paragraph on page 28, commencing on line 5, with the following amended paragraph:

In the HDR CDMA system, the transmitted traffic data is partitioned into a number of data streams, and each data stream is covered by a particular Walsh code. As defined by the HDR CDMA system, each Walsh code corresponds to a respective Walsh symbol having a length of (up to) 16 chips. To ~~channelized~~ channelize the data, each data bit is covered with the 16-chip Walsh symbol assigned to the channel on which the bit is transmitted. For each Walsh symbol period, up to 16 Walsh symbols for up to 16 data bits to be transmitted on up to 16 channels are generated and combined. The 16 Walsh symbols are orthogonal to one another and, in the absence of distortion, can be individually recovered at the receiver unit because the cross correlation between orthogonal sequences is (ideally) zero.

Please replace the paragraph on page 28, commencing on line 16, with the following amended paragraph:

FIG. 8A is a block diagram of a specific embodiment of symbol demodulator and combiner 524 within data processor 230. Pairs of correlated samples from correlator 522 are provided to a decover element 820 that decovers the samples with channelization (e.g., Walsh) symbols to provide decovered symbols. The decovered data symbols and the complex pilot symbols are provided to a pilot demodulator 850 that coherently ~~demodulate~~ demodulates the data with the pilot to generate demodulated symbols. The demodulated symbols are then provided to a symbol accumulator 870 and may be combined with other demodulated symbols from other signal paths or other redundant transmissions. The output from symbol accumulator 870 comprises the processed symbols that are then provided to buffer/de-interleaver 234 (see FIG. 5).

Please replace the paragraph on page 29, commencing on line 3, with the following amended paragraph:

Alternatively, FHT element 820 can be configured to decover the received samples with all N Walsh symbols. In this configuration, FHT element 820 performs the equivalent function of multiplying the N-by-N Hadamard matrix (corresponding to the N Walsh symbols, with each Walsh symbol having a length of N chips) by a vector comprising the N pairs of $I_{COR}$ and $Q_{COR}$ samples to generate N pairs of decovered $I_{DEC}$ and $Q_{DEC}$ symbols. Decovering with all N Walsh ~~symbol~~ symbols is especially advantageous, for example, in the HDR CDMA system in which data may be transmitted over more than one channel to a particular terminal.

Please replace the paragraph on page 32, commencing on line 30, with the following amended paragraph:

In the specific embodiment shown in FIG. 9, the correlated $I_{COR}$ and $Q_{COR}$ samples from correlator 522 are provided to a set of eight decover and accumulate elements 910a through 910h. Different number of decover and accumulate elements 910 can be used and are within the scope of the invention. Within each decover and accumulate element 910, the correlated $I_{COR}$ or $Q_{COR}$ samples are provided to an exclusive-OR gate 912 that also receives a Walsh symbol from a Walsh generator 914. Walsh generator 914 can be programmed to generate a particular Walsh symbol by loading the corresponding Walsh code in an associated latch 916. Thus, the eight decover and accumulate elements 910a through 910h can be programmed to perform decovering on a particular block of $I_{COR}$ and $Q_{COR}$ samples with eight different Walsh symbols.

Please replace the paragraph on page 33, commencing on line 7, with the following amended paragraph:

Within each decover and accumulate element 910, exclusive-OR gate 912 performs the decovering of the data samples with the Walsh symbol and provides the decovered samples to one input of a multiplexer 922. The other input of multiplexer 922 receives respective correlated samples (i.e., $I_{COR1}$, $I_{COR2}$, $Q_{COR1}$, or $Q_{COR2}$) from correlator 522. Depending on the particular task being performed, multiplexer 922 provides either the decovered samples from ~~multiplexer 922~~ exclusive-OR gate 912 or the correlated samples to a summer 924. Summer 924 also receives a previously latched sample from an ~~ADD~~ AND gate 926, sums the received samples,

and provides the accumulated output to a first set of registers 928a and 928b (coupled in series) and a second set of registers 930a and 930b (also coupled in series). The latched output from latch 928b and a control signal FLUSH/ are provided to the inputs of AND gate 926, which provides a value of zero to summer ~~926~~ 924 if the control signal FLUSH/ is low and the latched output if the control signal FLUSH/ is high. The latched output from latch 930b comprises the accumulated symbol, and is provided to one input of a multiplexer 940.

Please replace the paragraph on page 34, commencing on line 12, with the following amended paragraph:

In certain embodiments of the invention, micro-controller 232 is provided to receive tasks dispatched by controller 240 and to direct the operation of various elements of receiver unit 200 to execute the dispatched tasks. Each task can be defined to include a series of steps of operation or a number of other tasks. For example, a task may be dispatched to process a particular multipath at a particular time offset, to search for a strong signal instance within a particular time window, and so on. The search task may be achieved by directing correlator 522 and accumulator 526 to correlate a pilot signal over a particular time interval (e.g., 96 chips) at a specified PN offset. A task may also be dispatched to process all assigned multipaths, to search for strong signal instances at multiple time offsets, and so on. In an embodiment, micro-controller 232 instantiates an appropriate task state machine for each received task and maintains the task state machine for the duration of the task. Depending [[of]] on the particular task being processed, micro-controller 232 may further instantiate one or more additional task state machines for a lower hierarchical task. Micro-controller 232 may be configured to inform controller 240 when a particular task is completed.

Please replace the paragraph on page 34, commencing on line 29 and bridging pages 34 and 35, with the following amended paragraph:

The processing to be performed for search tasks, data processing tasks, signaling processing tasks, and other tasks are described in further detail in the following patents and

patent applications, all of which are assigned to the assignee of the present invention and incorporated herein by reference in their entirety:

1) U.S. Patent Nos. 5,644,591 and 5,805,648, both entitled "METHOD AND APPARATUS FOR PERFORMING SEARCH ACQUISITION IN A CDMA COMMUNICATIONS SYSTEM";
2) U.S. Patent Nos. 5,867,527 and 5,867,527, both entitled "METHOD OF SEARCHING FOR A BURSTY ~~SIGNAL";~~ SIGNAL;"
3) U.S. Patent No. 5,764,687, entitled "MOBILE DEMODULATOR ARCHITECTURE FOR A SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION ~~SIGNAL";~~ SIGNAL;"
4) U.S. Patent No. 5,577,022, entitled "PILOT SIGNAL SEARCHING TECHNIQUE FOR A CELLULAR COMMUNICATIONS ~~SIGNAL";~~ SIGNAL;"
5) U.S. Patent No. 5,654,979 entitled "CELL SITE DEMODULATION ARCHITECTURE FOR A SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION ~~SYSTEMS";~~ SYSTEMS;"
6) U.S. Patent Application Serial No. 08/987,172, entitled "MULTI CHANNEL ~~DEMODULATOR",~~ DEMODULATOR," filed December 9, 1997, now issued U.S. Patent No. 6,639,906, issued October 28, 2003 to Levin; and
7) U.S. Patent Application Serial No. 09/283,010, entitled "PROGRAMMABLE MATCHED FILTER ~~SEARCHER",~~ SEARCHER," filed March 31, 1999, now issued U.S. Patent No. 6,363,108, issued March 26, 2002 to Agrawal et al.

Please replace the paragraph on page 35, commencing on line 13, with the following amended paragraph:

FIG. 10 is a block diagram of a specific embodiment of micro-controller 232 that can be used to control the operation of the elements of receiver unit 200 (e.g., buffer 224 and data processor 230). Micro-controller 232 includes a sequencing controller 1012 ~~couples~~ coupled to a

counter 1014 and to latches 1016a and 1016b. Counter 1014 and latch 1016a further couple to latches 1016c and 1016d, respectively, which further couple to data bus 510.

Please replace the second paragraph on page 36, commencing on line 10, with the following amended paragraph:

In the first clock cycle, the complex PN samples for eight chips are retrieved from buffer 224 and provided to latch 732 within correlator [[732]] 522 (see FIG. 7A). In the second clock cycle, the data samples for the first two chips corresponding to time offsets of 0.0, 0.5, 1.0, and 1.5 are retrieved from buffer 224 and latched by latches 712a, 712b, 712c, and 712d, respectively. In the third clock cycles, the samples in latches 712 are re-latched by latches 714, and the data samples for the next two chips corresponding to time offsets of 2.0, 2.5, 3.0, and 3.5 are retrieved from buffer 224 and latched by latches 712a, 712b, 712c, and 712d, respectively. In the fourth clock cycle, the data samples for the first chip corresponding to time offsets of 0.0 and 0.5 are correlated by multipliers 720a and 720b, respectively, within correlator 522. In the fifth clock cycle, correlator 522 is idled. In the sixth clock cycle, the data samples for the second chip corresponding to time offsets of 1.0 and 1.5 are correlated by multipliers 720c and 720d, respectively. The processing performed for clock cycles seven through ten is similar to the processing performed for clock cycles three through six. The data processing further continues in similar manner until the next set of PN samples are needed and retrieved.